HIGH PERFORMANCE, SINGLE SYNCHRONOUS STEP-DOWN CONTROLLER FOR NOTEBOOK POWER SUPPLY

Check for Samples: TPS51217

FEATURES

- **Wide Input Voltage Range: 3 V to 28 V**
- **Output Voltage Range: 0.6 V to 2.6 V**
- **Wide Output Load Range: 0 to 20A+**
- **Built-in 0.5% 0.6 V Reference**
- **D-CAP™ Mode with 100-ns Load Step Response**
- **Adaptive On Time Control Architecture with Fixed 340kHz Operation**
- **Dynamic Output Voltage Change Capability**
- **4700 ppm/°C $R_{DS(on)}$ Current Sensing**
- **Internal 0.9-ms Voltage Servo Softstart**
- **Pre-Charged Start-up Capability**
- **Built-in Output Discharge**
- **Power Good Output**
- **Integrated Boost Switch**
- **Built-in OVP/UVP/OCP**
- **Thermal Shutdown (Non-latch)**
- **SON-10 (DSC) Package**

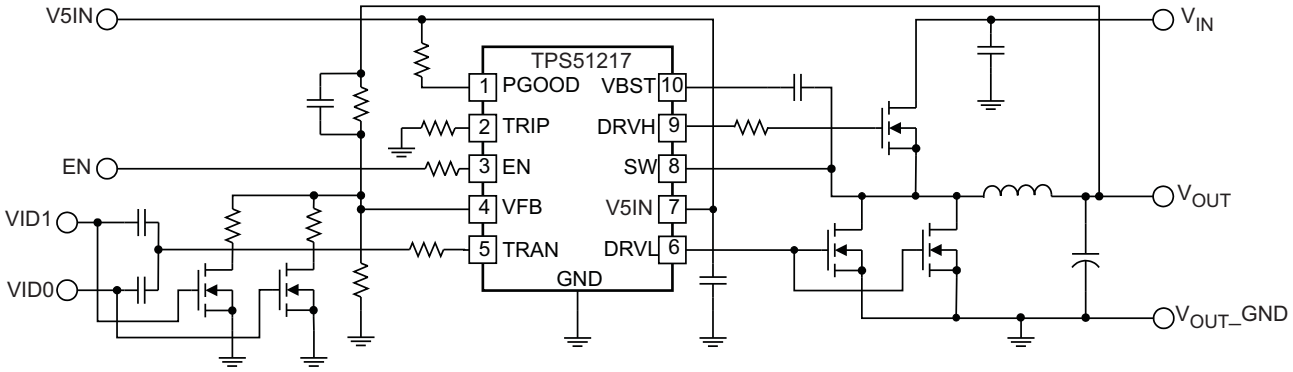
APPLICATIONS

- **Notebook Computers**
- **I/O Supplies**
- **System Power Supplies**

DESCRIPTION

The TPS51217 is a small-sized single buck controller with adaptive on-time D-CAP™ mode. The device is suitable for low output voltage, high current, PC system power rail and similar point-of-load (POL) power supply in digital consumer products. A small package with minimal pin-count saves space on the PCB, while a dedicated EN pin and pre-set frequency minimize design effort required for new designs. The skip-mode at light load condition, strong gate drivers and low-side FET $R_{DS(on)}$ current sensing supports low-loss and high efficiency, over a broad load range. The TRAN pin provides freedom of masking overvoltage protection, undervoltage protection and power-good signal during the transition period of dynamic output voltage change for modern GPU power supply applications. The conversion input voltage which is the high-side FET drain voltage ranges from 3 V to 28 V and the output voltage ranges from 0.6 V to 2.6 V. The device requires an external 5-V supply. The TPS51217 is available in a 10-pin SON package specified from –40°C to 85°C.

TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

T_A	PACKAGE	ORDERING DEVICE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY
–40°C to 85°C	Plastic SON PowerPAD	TPS51217DSCR	10	Tape and reel	3000
		TPS51217DSCT	10	Mini reel	250

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		
		MIN	MAX	UNIT
Input voltage range(2)	VBST	–0.3	37	V
	VBST(3)	–0.3	7	
	SW	–5	30	
	V5IN, EN, TRIP, VFB, TRAN	–0.3	7	
Output voltage range(2)	DRVH	–5	37	V
	DRVH(3)	–0.3	7	
	DRVH(3), pulse wiidth < 20 ns	–2.5	7	
	DRVL	–0.5	7	
	DRVL, pulse width < 20 ns	–2.5	7	
	PGOOD	–0.3	7	
Junction temperature range, T_J			150	°C
Storage temperature range, T_{STG}		–55	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the SW terminal.

DISSIPATION RATINGS

2-oz. trace and copper pad with solder.

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
10 pin DSC(1)	1.54 W	15 mW/°C	0.62 W

(1) Enhanced thermal conductance by thermal vias is used beneath thermal pad as shown in Land Pattern information.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Supply voltage	V5IN	4.5		6.5	V
Input voltage range	VBST	–0.1		34.5	V
	SW	–1		28	
	SW(1)	–4		28	
	VBST(2)	–0.1		6.5	
	EN, TRIP, VFB, TRAN	–0.1		6.5	
Output voltage range	DRVH	–1		34.5	V
	DRVH(1)	-4		34.5	
	DRVH(2)	–0.1		6.5	
	DRVL	–0.3		6.5	
	PGOOD	–0.1		6.5	
Operating free-air temperature, T_A		–40		85	°C

(1) This voltage should be applied for less than 30% of the repetitive period.
(2) Voltage values are with respect to the SW terminal.

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, V5IN = 5V. (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{(V5IN)}$	V5IN supply current	V5IN current, T_A = 25°C, No Load, $V_{(EN)}$ = 5 V, $V_{(VFB)}$ = 0.63 V		320	500	µA
$I_{SD(V5IN)}$	V5IN shutdown current	V5IN current, T_A = 25°C, No Load, $V_{(EN)}$ = 0 V			1	µA
INTERNAL REFERENCE VOLTAGE						
$V_{(VFB)}$	VFB regulation voltage	VFB voltage, CCM condition(1)		0.6000		V
		T_A = 25°C, skip mode	0.6000	0.6030	0.6060	V
		T_A = 0°C to 85°C, skip mode	0.5974	0.6030	0.6086	
		T_A = –40°C to 85°C, skip mode	0.5960	0.6030	0.6100	
$I_{(VFB)}$	VFB input current	$V_{(VFB)}$ = 0.63 V, T_A = 25°C, skip mode		0.01	0.2	µA
OUTPUT DISCHARGE						
I_{Dischg}	Output discharge current from SW pin	$V_{(EN)}$ = 0 V, $V_{(SW)}$ = 0.5 V	5	13		mA
OUTPUT DRIVERS						
$R_{(DRVH)}$	DRVH resistance	Source, $I_{(DRVH)}$ = –50 mA		1.5	3	Ω
		Sink, $I_{(DRVH)}$ = 50 mA		0.7	1.8	
$R_{(DRVL)}$	DRVL resistance	Source, $I_{(DRVL)}$ = –50 mA		1.0	2.2	
		Sink, $I_{(DRVL)}$ = 50 mA		0.5	1.2	
t_D	Dead time	DRVH-off to DRVL-on	7	17	30	ns
		DRVL-off to DRVH-on	10	22	35	
BOOT STRAP SWITCH						
$V_{(FBST)}$	Forward voltage	$V_{(V5IN-VBST)}$, I_F = 10 mA, T_A = 25°C		0.1	0.2	V
I_{lkg}	VBST leakage current	$V_{(VBST)}$ = 34.5 V, $V_{(SW)}$ = 28 V, T_A = 25°C		0.01	1.5	µA
DUTY AND FREQUENCY CONTROL						
$t_{OFF(min)}$	Minimum off-time	T_A = 25°C	150	260	400	ns
$t_{ON(min)}$	Minimum on-time	V_{IN} = 28 V, V_{OUT} = 0.6 V, T_A = 25°C(1)		86		
f_{SW}	Switching frequency	T_A = 25°C(2)	312	340	368	kHz

(1) Specified by design. Not production tested.
(2) Not production tested. Test condition is V_{IN} = 8 V, V_{OUT} = 1.1 V, I_{OUT} = 10A using the application circuit shown in Figure 26.

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, V5IN = 5V. (Unless otherwise noted)

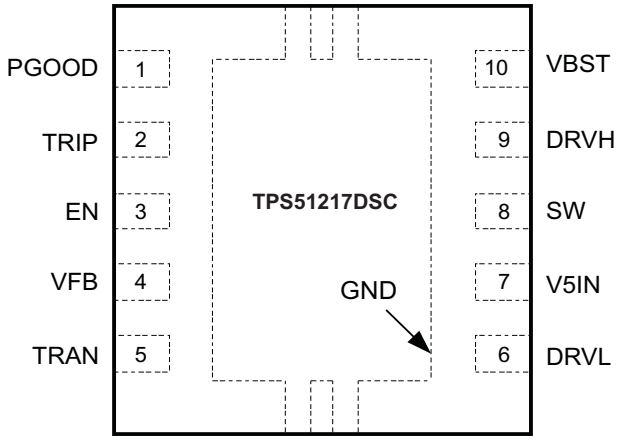
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOFTSTART						
t_{SS}	Internal soft-start time	From $V_{(EN)}$ = high to V_{OUT} = 95%		0.9		ms
POWERGOOD						
$V_{(THPG)}$	PG threshold	PG in from lower	92.5%	95%	97.5%	
		PG in from higher	107.5%	110%	112.5%	
		PG hysteresis	2.5%	5%	7.5%	
$I_{(PG)max}$	PG sink current	$V_{(PGOOD)}$ = 0.5 V	3	6		mA
t_{PGDEL}	PG delay	Delay for PG in	0.8	1	1.2	ms
LOGIC THRESHOLD AND SETTING CONDITIONS						
$V_{(EN)}$	EN voltage	Enable	1.8			V
		Disable			0.5	
$I_{(EN)}$	EN input current	$V_{(EN)}$ = 5V			1.0	µA
$V_{(TRAN)}$	TRAN voltage	TRAN open	1.83	1.88	1.93	V
		Mask PG, OVP and UVP, high side	2.03	2.08	2.13	
		Mask PG, OVP and UVP, low side	1.62	1.67	1.72	
		Hysteresis		0.05		
$I_{(TRAN)}$	TRAN input current	$V_{(TRAN)}$ = 5 V, T_A = 25°C	2.5	3.8	5	µA
		$V_{(TRAN)}$ = 0 V, T_A = 25°C	–5	–3.8	–2.5	
PROTECTION: CURRENT SENSE						
$I_{(TRIP)}$	TRIP source current	$V_{(TRIP)}$ = 1V, T_A = 25°C	9	10	11	µA
	TRIP current temperature coefficient	On the basis of 25°C		4700		ppm/°C
$V_{(TRIP)}$	Current limit threshold setting range	$V_{(TRIP-GND)}$ voltage	0.2		3	V
V_{OCL}	Current limit threshold	$V_{(TRIP)}$ = 3 V	355	375	395	mV
		$V_{(TRIP)}$ = 1.6 V	185	200	215	
		$V_{(TRIP)}$ = 0.2 V	17	25	33	
V_{OCLN}	Negative current limit threshold	$V_{(TRIP)}$ = 3 V	–395	–375	–355	mV
		$V_{(TRIP)}$ = 1.6 V	–215	–200	–185	
		$V_{(TRIP)}$ = 0.2 V	–33	–25	–17	
V_{AZCADJ}	Adaptive zero cross adjustable range	Positive	3	15		mV
		Negative		–15	–3	
PROTECTION: UVP AND OVP						
$V_{(OVP)}$	OVP trip threshold	OVP detect	115%	120%	125%	
t_{OVPDEL}	OVP propagation delay time	50-mV overdrive		1		µs
$V_{(UVP)}$	Output UVP trip threshold	UVP detect	65%	70%	75%	
t_{UVPDEL}	Output UVP propagation delay		0.8	1	1.2	ms
t_{UVPEN}	Output UVP enable delay time	From Enable to UVP workable	1	1.2	1.4	ms
UVLO						
	V5IN UVLO threshold	Wake up	4.20	4.38	4.50	V
		Shutdown	3.7	3.93	4.1	
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature (3)		145		°C
		Hysteresis (3)		10		

(3) Specified by design. Not production tested.

DEVICE INFORMATION

DSC PACKAGE

(TOP VIEW)

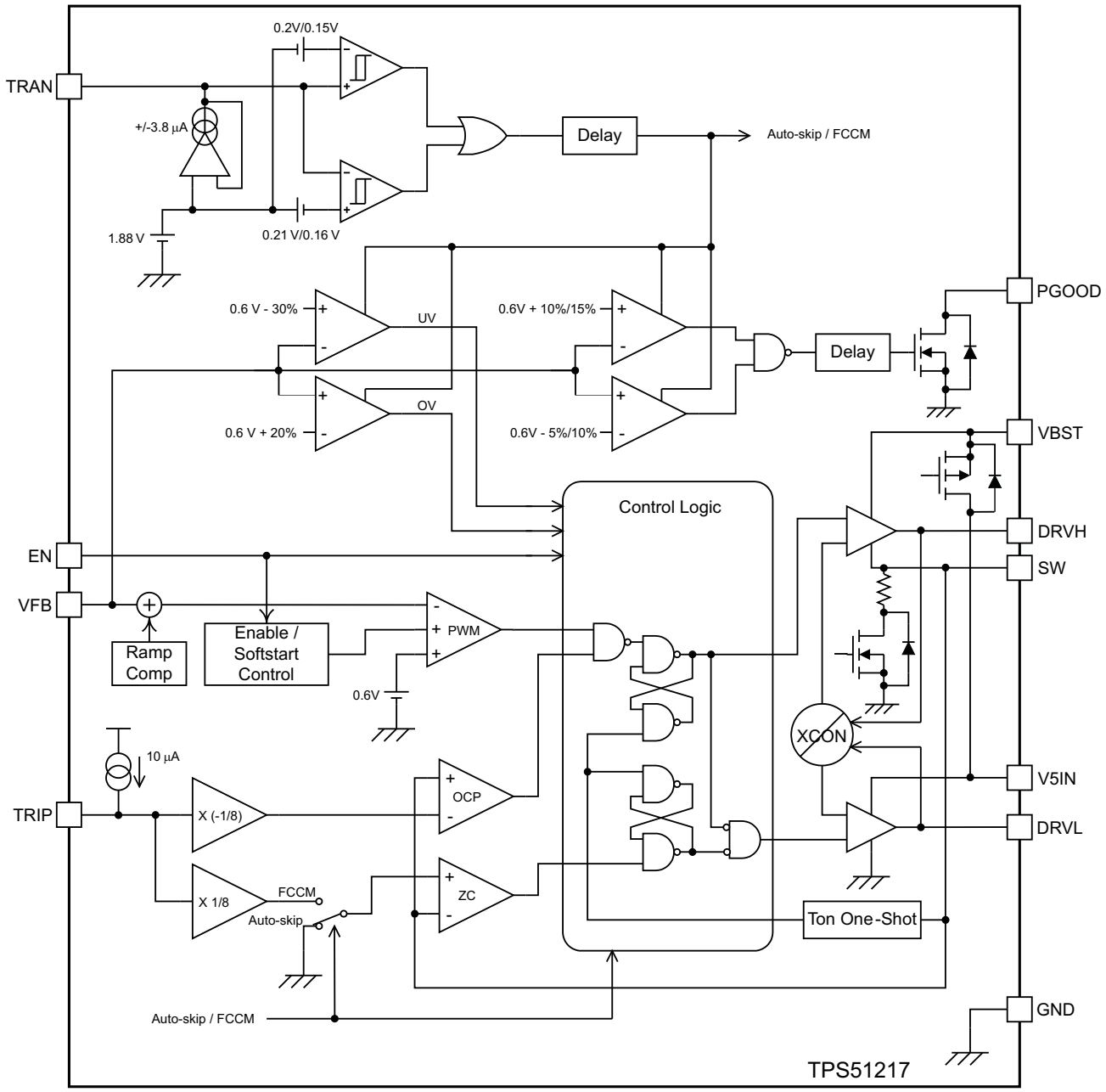


Thermal pad is used as an active terminal of GND.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
DRVH	9	O	High-side MOSFET driver output. The SW node referenced floating driver. The gate drive voltage is defined by the voltage across VBST to SW node bootstrap flying capacitor
DRVL	6	O	Synchronous MOSFET driver output. The GND referenced driver. The gate drive voltage is defined by V5IN voltage.
EN	3	I	SMPS enable pin. Short to GND to disable the device.
GND	Thermal Pad	I	Ground
PGOOD	1	O	Power Good window comparator open drain output. Pull up with resistor to 5 V or appropriate signal voltage. Continuous current capability is 1 mA. PGOOD goes high 1 ms after VFB becomes within specified limits. Power bad, or the terminal goes low, after a 2- µs delay.
SW	8	I	Switch node. A high-side MOSFET gate drive return. Also used for on time generation and output discharge.
TRAN	5	I	Dynamic voltage change control. It forces CCM and masks PGOOD, OVP and UVP when this pin's status is pulled up or pulled down. The masking is terminated 900 µs after TRAN pin voltage returns to normal. See the DYNAMIC VOLTAGE STEP and PGOOD/OVP/UVP MASK section for a detailed description. Leave this pin open when dynamic voltage change is not used.
TRIP	2	I	OCL detection threshold setting pin. 10 µA at room temperature, 4700 ppm/°C current is sourced and set the OCL trip voltage as follows. $V_{OCL} = \frac{V_{(TRIP)}}{8}$ $(0.2\ V \le V_{(TRIP)} \le 3\ V)$
V5IN	7	I	5 V +30% / –10% power supply input.
VBST	10	I	Supply input for high-side MOSFET driver (bootstrap terminal). Connect a flying capacitor from this pin to the SW pin. Internally connected to V5IN via bootstrap MOSFET switch.
VFB	4	I	SMPS feedback input. Connect the feedback resistor divider.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

V5IN SUPPLY CURRENT vs JUNCTION TEMPERATURE

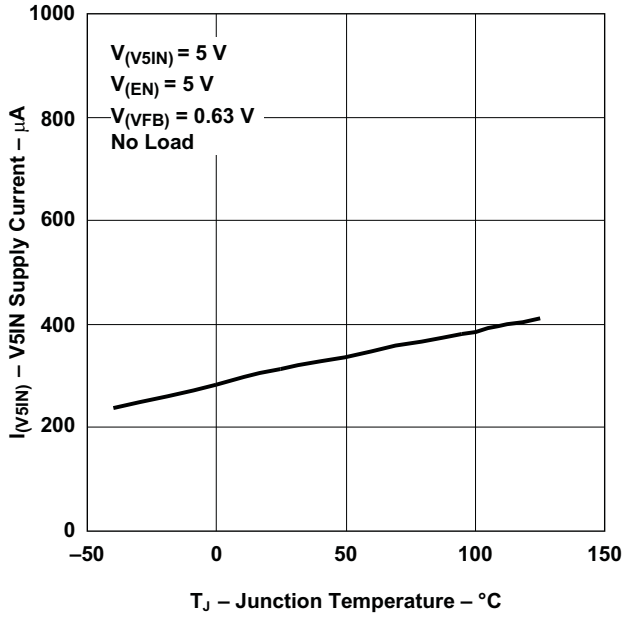


Figure 1.

V5IN SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

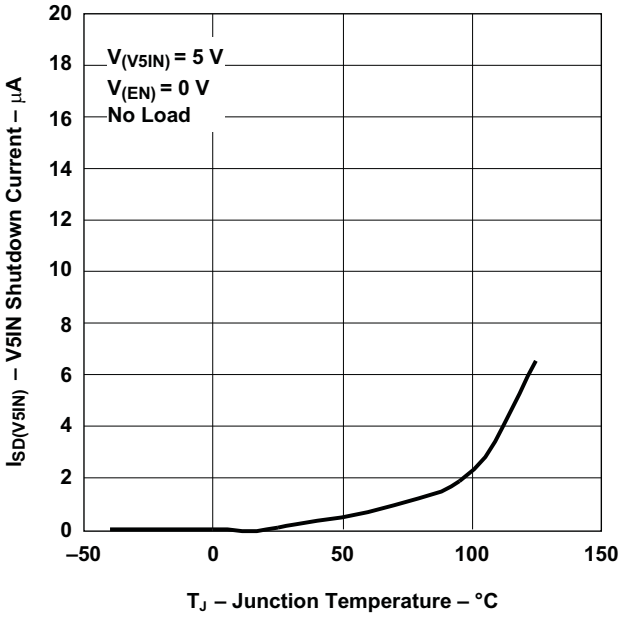


Figure 2.

OVP/UVP THRESHOLD vs JUNCTION TEMPERATURE

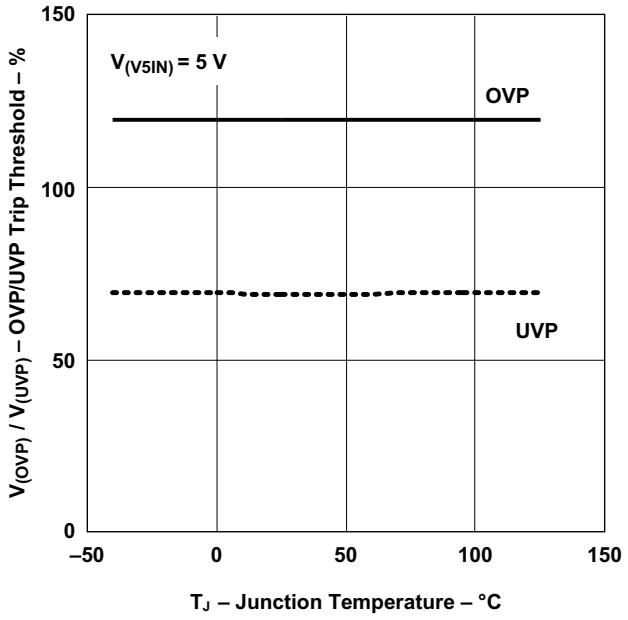


Figure 3.

CURRENT SENSE CURRENT, $I_{(TRIP)}$ vs JUNCTION TEMPERATURE

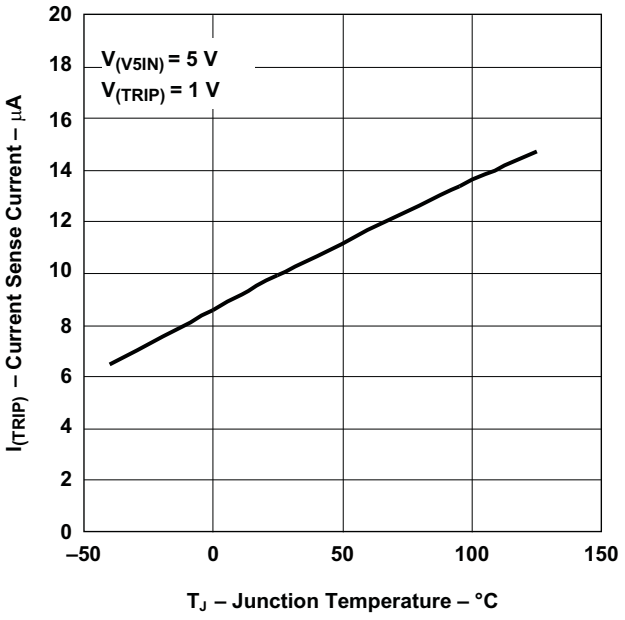


Figure 4.

TYPICAL CHARACTERISTICS (continued)

TRAN INPUT CURRENT, $I_{(TRAN)}$ vs JUNCTION TEMPERATURE

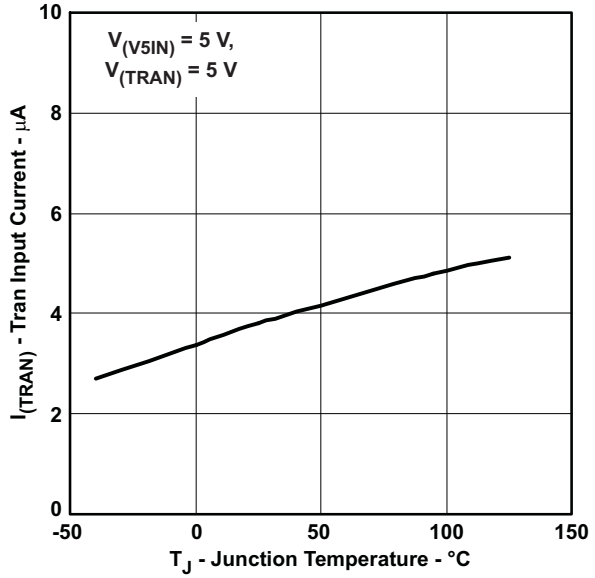


Figure 5.

TRAN INPUT CURRENT, $I_{(TRAN)}$ vs JUNCTION TEMPERATURE

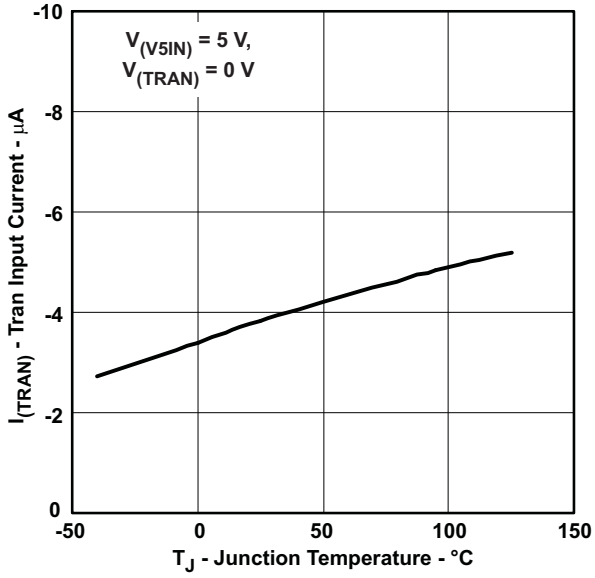


Figure 6.

SWITCHING FREQUENCY vs INPUT VOLTAGE

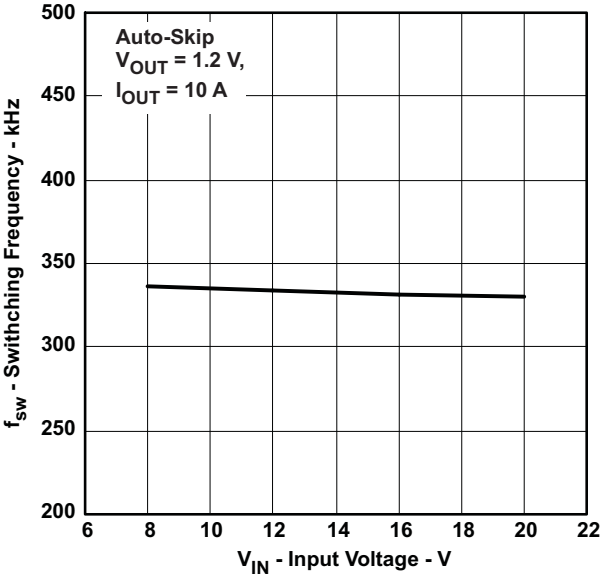


Figure 7.

SWITCHING FREQUENCY vs OUTPUT CURRENT

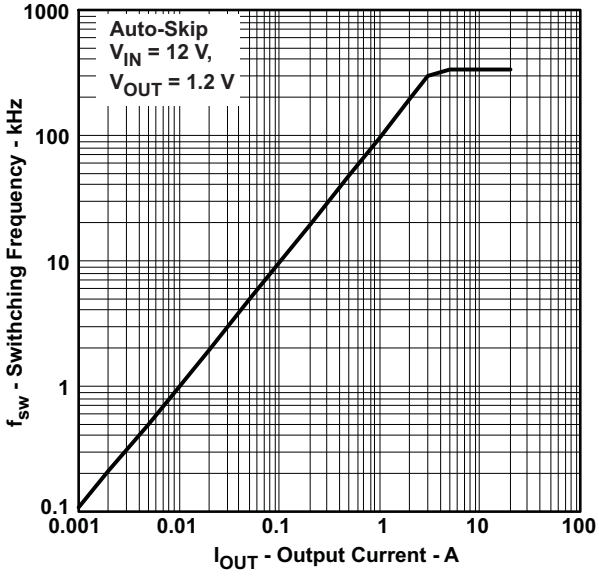


Figure 8.

TYPICAL CHARACTERISTICS (continued)

0.9-V OUTPUT VOLTAGE vs OUTPUT CURRENT

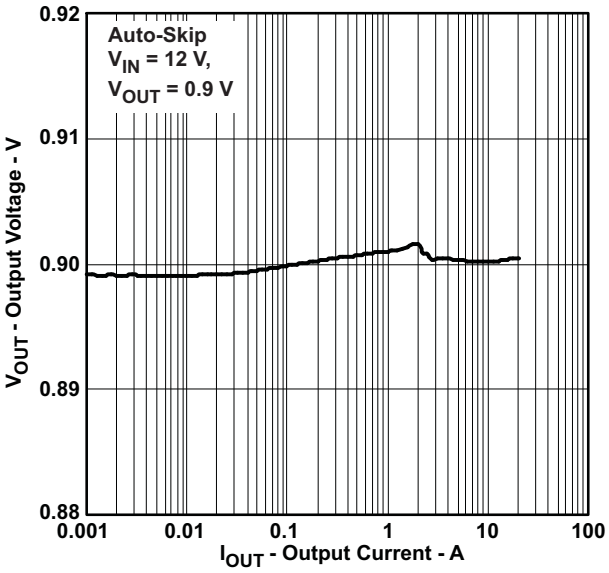


Figure 9.

1.2-OUTPUT VOLTAGE vs OUTPUT CURRENT

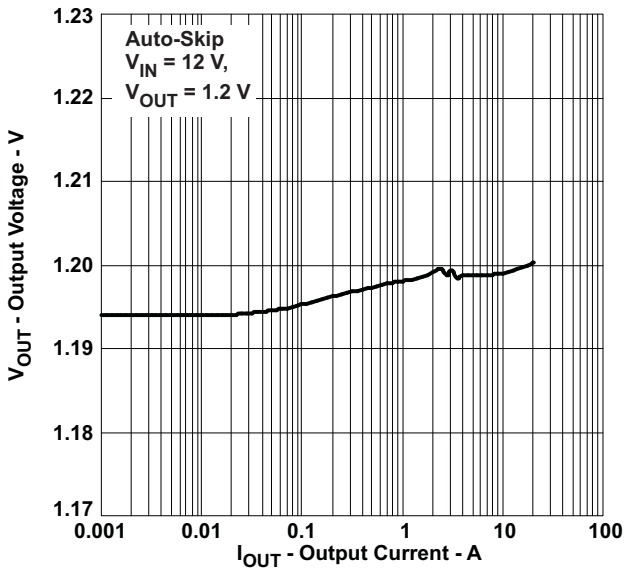


Figure 10.

0.9-OUTPUT VOLTAGE vs INPUT VOLTAGE

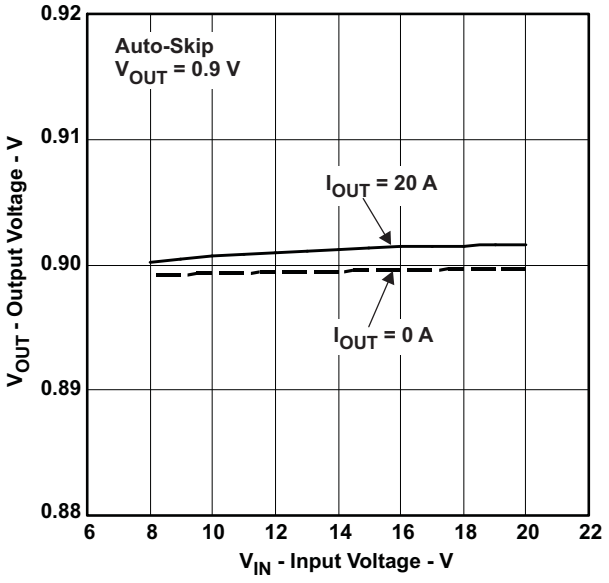


Figure 11.

1.2-V OUTPUT VOLTAGE vs INPUT VOLTAGE

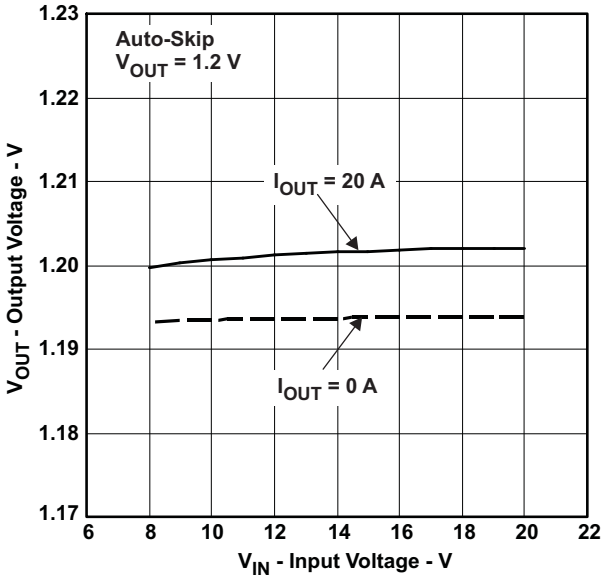


Figure 12.

TYPICAL CHARACTERISTICS (continued)

0.9-V EFFICIENCY vs OUTPUT CURRENT

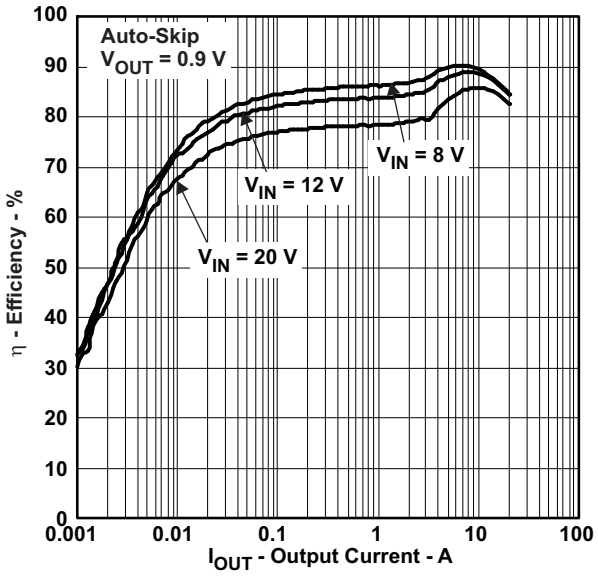


Figure 13.

1.2-V EFFICIENCY vs OUTPUT CURRENT

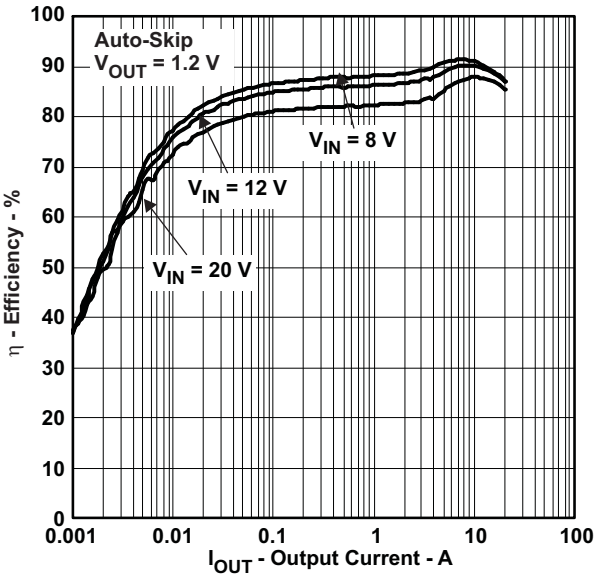


Figure 14.

0.9-V START-UP WAVEFORM

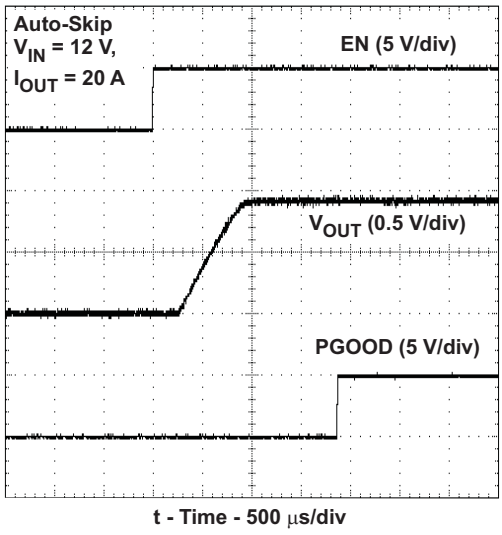


Figure 15.

PRE-BIASED START-UP WAVEFORM

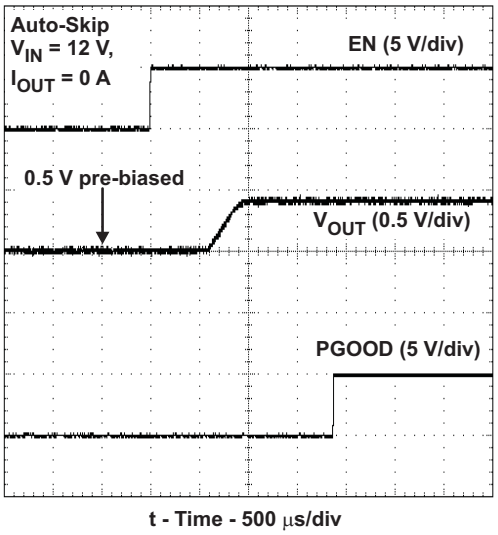
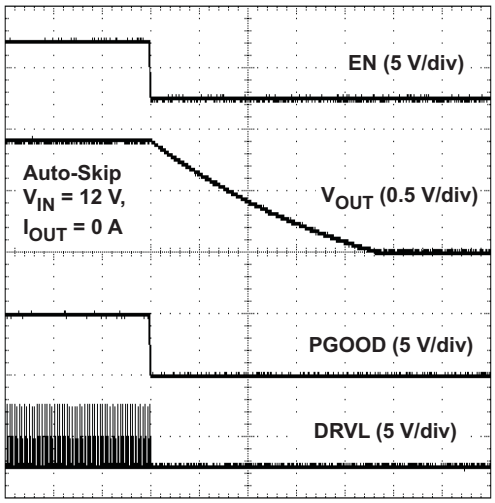


Figure 16.

TYPICAL CHARACTERISTICS (continued)

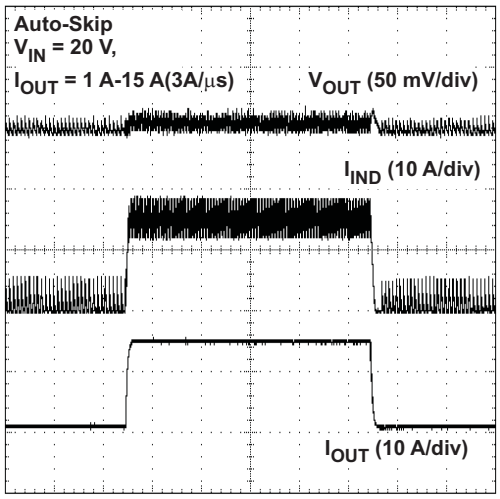
0.9-V SOFT-STOP WAVEFORM



t - Time - 10 ms/div

Figure 17.

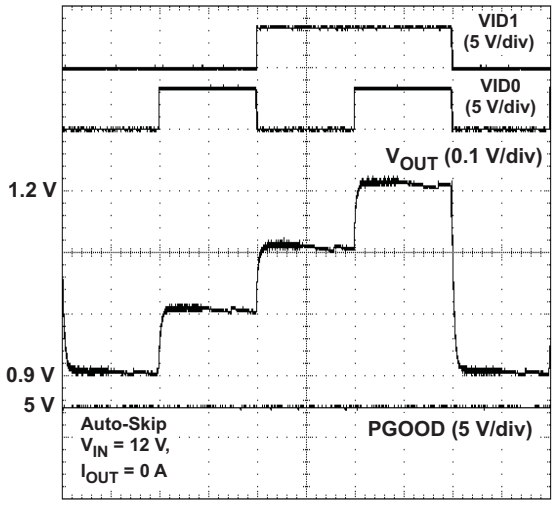
0.9-V LOAD TRANSIENT RESPONSE



t - Time - 100 μs/div

Figure 18.

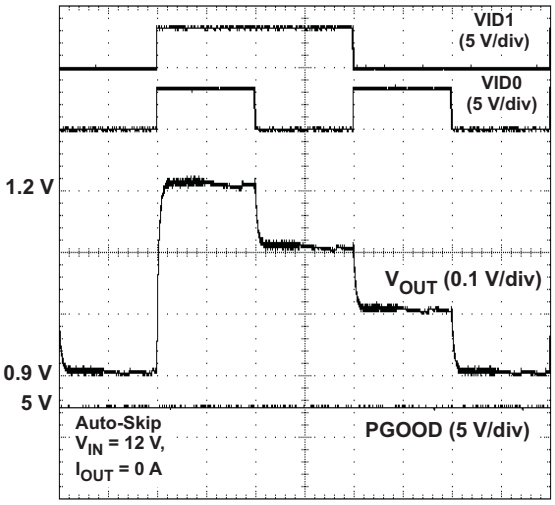
DYNAMIC OUTPUT VOLTAGE TRANSITION



t - Time - 1 ms/div

Figure 19.

DYNAMIC OUTPUT VOLTAGE TRANSITION



t - Time - 1 ms/div

Figure 20.

APPLICATION INFORMATION

GENERAL DESCRIPTION

The TPS51217 is a high-efficiency, single channel, synchronous buck regulator controller suitable for low output voltage point-of-load applications in notebook computers and similar digital consumer applications. The device features proprietary D-CAP™ mode control combined with adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC/DC converters. The output voltage ranges from 0.6 V to 2.6 V. The conversion input voltage range is from 3 V to 28 V. The D-CAP™ mode uses the ESR of the output capacitor(s) to sense current information. An advantage of this control scheme is that it does not require an external phase compensation network, helping the designer with ease-of-use and realizing low external component count configuration. Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages, while it increases the switching frequency at step-up of load.

The strong gate drivers of the TPS51217 allow low $R_{DS(on)}$ FETs for high current applications.

ENABLE AND SOFT START

When the EN pin voltage rises above the enable threshold, (typically 1.2 V) the controller enters its start-up sequence. The first 250 µs is a standby phase. Switching is inhibited during this phase. In the second phase, internal DAC starts ramping up the reference voltage from 0 V to 0.6 V. This ramping time is 650 µs. Smooth and constant ramp up of the output voltage is maintained during start up regardless of load current. Connect a 1-kΩ resistor in series with the EN pin to provide protection.

ADAPTIVE ON-TIME D-CAP™ CONTROL

TPS51217 does not have a dedicated oscillator that determines switching frequency. However, the device runs with pseudo-constant frequency by feed-forwarding the input and output voltages into its on-time one-shot timer. The adaptive on-time control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage ($t_{ON} \propto V_{OUT} / V_{IN}$). This makes the switching frequency fairly constant in steady state conditions over wide input voltage range.

The off-time is modulated by a PWM comparator. The VFB node voltage (the mid point of resistor divider) is compared to the internal 0.6-V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts the *set* signal to terminate the off-time (turn off the low-side MOSFET and turn on high-side MOSFET). The set signal becomes valid if the inductor current level is below OCP threshold, otherwise the off-time is extended until the current level to become below the threshold.

SMALL SIGNAL MODEL

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in Figure 21.

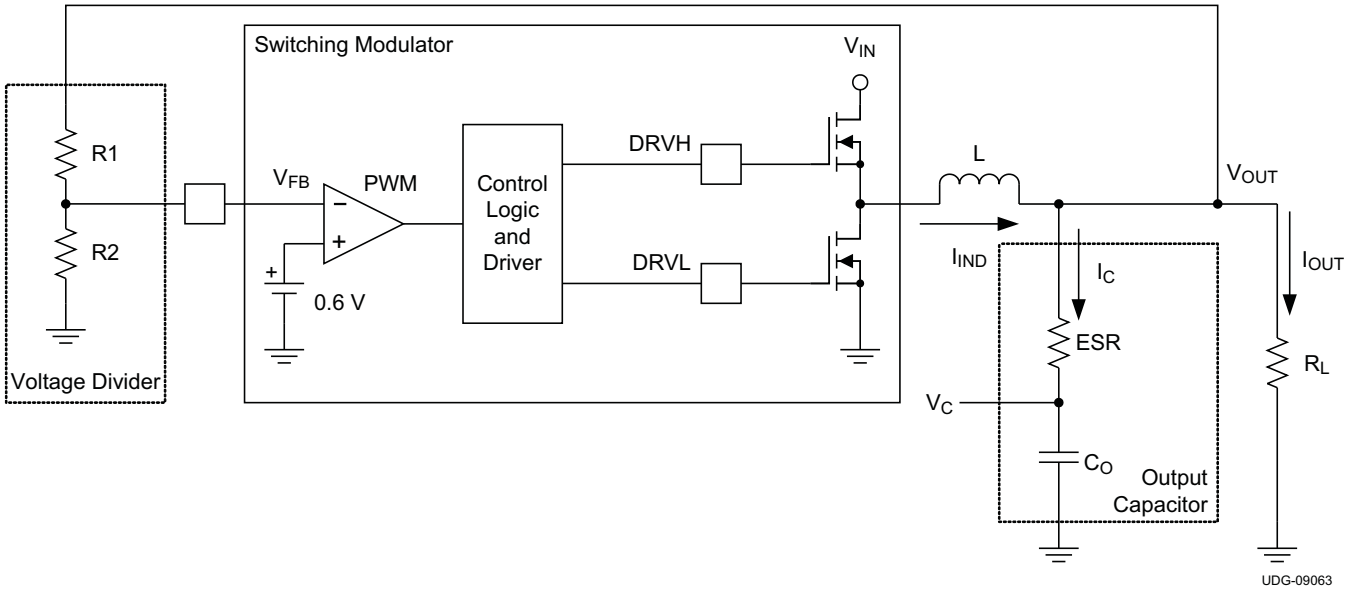


Figure 21. Simplified Modulator Model

The output voltage is compared with internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each on cycle substantially constant.

$$H(s) = \frac{1}{s \times ESR \times C_O} \tag{1}$$

For loop stability, the 0-dB frequency, f_0, defined in Equation 2 need to be lower than 1/4 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_O} \le \frac{f_{SW}}{4} \tag{2}$$

According to Equation 2, the loop stability of D-CAP™ mode modulator is mainly determined by the capacitor's chemistry. For example, specialty polymer capacitors (SP-CAP) have C_O on the order of several 100 µF and ESR in range of 10 mΩ. These makes f_0 on the order of 100 kHz or less and the loop is stable. However, ceramic capacitors have an f_0 of more than 700 kHz, which is not suitable for this modulator.

RAMP SIGNAL

The TPS51217 adds a ramp signal to the 0.6-V reference in order to improve its jitter performance. As described in the previous section, the feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the S/N ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with –6 mV at the beginning of ON-cycle and becomes 0 mV at the end of OFF-cycle in continuous conduction steady state.

LIGHT LOAD CONDITION IN AUTO-SKIP OPERATION

The TPS51217 automatically reduces switching frequency at light load conditions to maintain high efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled *valley* touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs in to discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{O(LL)}$ (i.e., the threshold between continuous and discontinuous conduction mode) can be calculated in Equation 3.

$$I_{O(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (3)$$

where

- f_{SW} is the PWM switching frequency (340 kHz)

Switching frequency versus output current in the light load condition is a function of L, V_{IN} and V_{OUT}, but it decreases almost proportional to the output current from the $I_{O(LL)}$ given in Equation 3. For example, it is 68 kHz at $I_{O(LL)}/5$.

ADAPTIVE ZERO CROSSING

The TPS51217 has an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the ZC comparator and delay time of the ZC detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

OUTPUT DISCHARGE CONTROL

When EN is low, the TPS51217 discharges the output capacitor using internal MOSFET connected between SW and GND while high-side and low-side MOSFETs are kept off. The current capability of this MOSFET is limited to discharge slowly.

LOW-SIDE DRIVER

The low-side driver is designed to drive high current low $R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance, which are 1.0Ω for V5IN to DRVL and 0.5Ω for DRVL to GND. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. 5-V bias voltage is delivered from V5IN supply. The instantaneous drive current is supplied by an input capacitor connected between V5IN and GND. The average drive current is equal to the gate charge at Vgs=5V times switching frequency. This gate drive current as well as the high-side gate drive current times 5V makes the driving power which need to be dissipated from TPS51217 package.

HIGH-SIDE DRIVER

The high-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFET(s). When configured as a floating driver, 5 V of bias voltage is delivered from V5IN supply. The average drive current is also equal to the gate charge at Vgs = 5V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between VBST and SW pins. The drive capability is represented by its internal resistance, which are 1.5 Ω for VBST to DRVH and 0.7 Ω for DRVH to SW.

POWER-GOOD

The TPS51217 has powergood output that indicates high when switcher output is within the target. The powergood function is activated after soft-start has finished. If the output voltage becomes within +10%/–5% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of +15%/–10% of the target value, the powergood signal becomes low after a 2-µs internal delay. The powergood output is an open-drain output and must be pulled up externally.

CURRENT SENSE AND OVERCURRENT PROTECTION

TPS51217 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the OFF state and the controller keeps the OFF state during the inductor current is larger than the overcurrent trip level. To provide both good accuracy and cost effective solution, the TPS51217 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, $R_{(TRIP)}$. The TRIP terminal sources $I_{(TRIP)}$ current, which is 10µA typically at room temperature, and the trip level is set to the OCL trip voltage $V_{(TRIP)}$ as shown in Equation 4. Note that $V_{(TRIP)}$ is limited up to approximately 3 V internally.

$$V_{(TRIP)}(mV) = R_{(TRIP)}(k\Omega) \times I_{(TRIP)}(\mu A) \quad (4)$$ (4)

The inductor current is monitored by the voltage between GND pad and SW pin so that the SW pin should be connected to the drain terminal of the low-side MOSFET properly. $I_{(TRIP)}$ has 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. GND is used as the positive current sensing node so that GND should be connected to the proper current sensing device, i.e. the source terminal of the low-side MOSFET.

As the comparison is done during the OFF state, $V_{(TRIP)}$ sets valley level of the inductor current. Thus, the load current at overcurrent threshold, I_{OCP}, can be calculated in Equation 5

$$I_{OCP} = \left(\frac{V_{(TRIP)}}{8 \times R_{DS(on)}} \right) + \frac{I_{IND(ripple)}}{2} = \frac{V_{(TRIP)}}{8 \times R_{DS(on)}} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (5)$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. Eventually, it crosses the undervoltage protection threshold and shuts down the controller.

When the device is operating in the forced continuous conduction mode, the negative current limit (NCL) protects the external FET from carrying too much current. The NCL detect threshold is set as the same absolute value as positive OCL but negative polarity. Note that the forced continuous conduction mode appears only during the Dynamic Voltage Step operation, and the threshold still represents the valley value of the inductor current.

OVER/UNDER VOLTAGE PROTECTION

TPS51217 monitors a resistor divided feedback voltage to detect over and undervoltage. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches as the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After a 1-ms delay, TPS51217 latches OFF both high-side and low-side MOSFETs drivers. This function is enabled after 1.2 ms following EN has become high.

DYNAMIC VOLTAGE STEP and PGOOD/OVP/UVP MASK

Output voltage of switcher can be dynamically step-up or step-down by controlling bottom resistance of the output voltage divider. The simplest way is to add a MOSFET switch plus a resistor in parallel with the bottom resistor. When the MOSFET switch is turned on, the VFB voltage is immediately dropped and comes back equivalent to the internal reference voltage as the output voltage climbs up to match the new target. If the voltage step is large, it may cause PGOOD state into 'bad' and also may hit UVP. In the case of voltage step-down, the same PGOOD bad and OVP hit may happen. TRAN pin helps masking PGOOD, UVP and OVP during the voltage transition. Combination of weighted capacitances C2 and C3 detect transition of VIDx (Figure 22). Masking of PGOOD, OVP and UVP start when the TRAN pin voltage goes outside of its window comparator threshold. At this time, TRAN pin also starts sink or source current. 900µsec after TRAN pin voltage recovers

within the threshold window, PGOOD, OVP and UVP are released from masking. The TRAN pin operation is useful for graphics power applications such that switcher output voltage needs to be changed dynamically. At the transition of output voltage, inductor current has a chance to hit over current limit (OCL) to quickly charge the output capacitor, which may cause output voltage undershoot or overshoot. Capacitance C1 in parallel with the top resistor slows down transition slew rate and prevent from hitting OCL. Time constant of the transition is R1 × C1. From 3.3 V to 5 V is recommended for VIDx input amplitude.

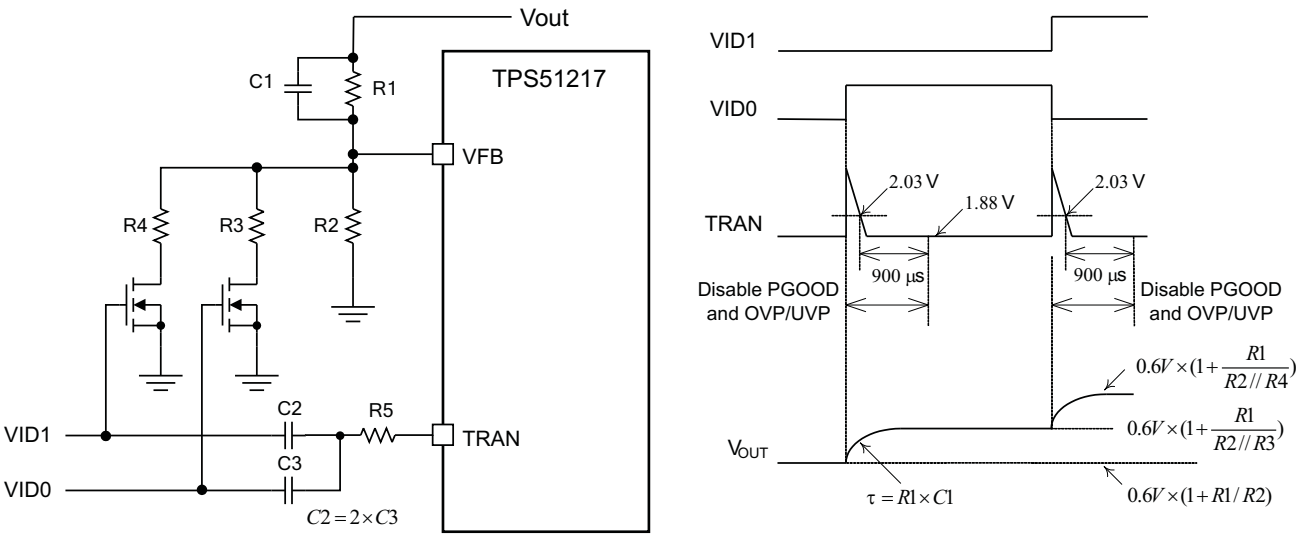


Figure 22. Dynamic Voltage Step Application

UVLO PROTECTION

TPS51217 has V5IN undervoltage lockout protection (UVLO). When the V5IN voltage is lower than UVLO threshold voltage, the switch mode power supply shuts off. This is non-latch protection.

THERMAL SHUTDOWN

TPS51217 monitors the die temperature. If the temperature exceeds the threshold value (typically 145°C), the TPS51217 is shut off. This is non-latch protection.

EXTERNAL COMPONENTS SELECTION

Selecting external components is simple in D-CAP™ mode.

1. Choose the inductor.

The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves S/N ratio and helps stable operation.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (6)$$

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated in Equation 7.

$$I_{IND(peak)} = \frac{V_{(TRIP)}}{8 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (7)$$

2. Choose the output capacitor(s).

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. For loop stability, capacitance and ESR should satisfy Equation 2. For jitter performance, Equation 8 is a good starting point to determine ESR.

$$ESR = \frac{V_{OUT} \times 10[mV] \times (1\text{-}D)}{0.6[V] \times I_{IND(ripple)}} = \frac{10[mV] \times L \times f_{SW}}{0.6[V]} = \frac{L \times f_{SW}}{60}[\Omega] \quad (8)$$

where

- D is the duty ratio
- the output ripple down slope rate is 10 mV/t_{SW} in terms of VFB terminal voltage as shown in Figure 23
- t_{SW} is the switching period

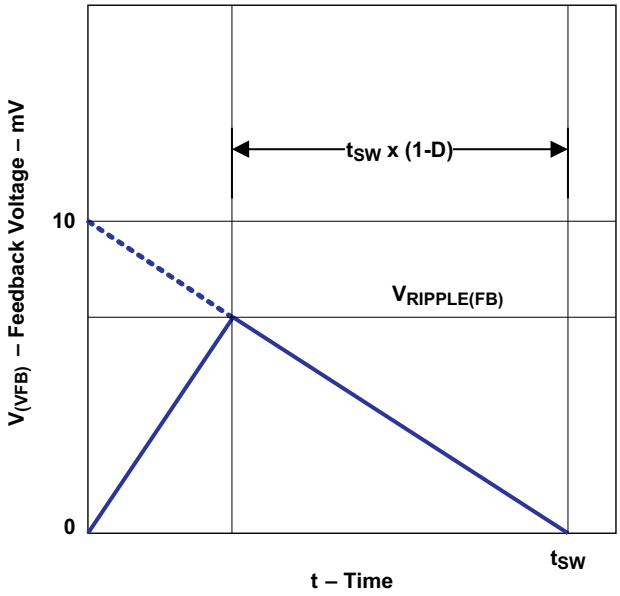


Figure 23. Ripple Voltage Down Slope

3. Determine the value of R1 and R2.

The output voltage is programmed by the voltage-divider resistor, R1 and R2, shown in Figure 21. R1 is connected between the VFB pin and the output, and R2 is connected between the VFB pin and GND. Typical designs begin with the selection of an R2 value between 10 kΩ and 20 kΩ. Determine R1 using Equation 9.

$$R1 = \frac{\left(V_{OUT} - \frac{I_{IND(ripple)} \times ESR}{2}\right) - 0.6}{0.6} \times R2 \quad (9)$$

LAYOUT CONSIDERATIONS

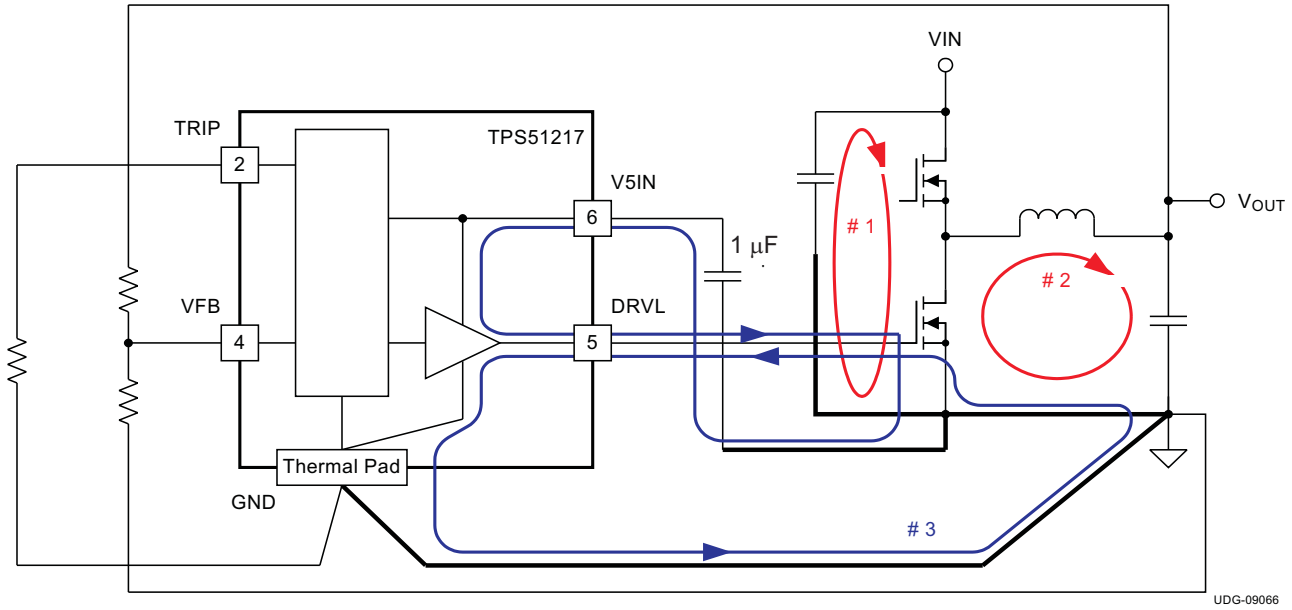


Figure 24. Ground System of DC/DC Converter Using the TPS51217

Certain points must be considered before starting a layout work using the TPS51217.

- Inductor, V_{IN} capacitor(s), V_{OUT} capacitor(s) and MOSFETs are the power components and should be placed on one side of the PCB (solder side). Other small signal components should be placed on another side (component side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP and TRAN should be placed away from high-voltage switching nodes such as SW, DRVL, DRVH or VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- The DC/DC converter has several high-current loops. The area of these loops should be minimized in order to suppress generating switching noise.
  - The most important loop to minimize the area of is the path from the V_{IN} capacitor(s) through the high and low-side MOSFETs, and back to the capacitor(s) through ground. Connect the negative node of the V_{IN} capacitor(s) and the source of the low-side MOSFET at ground as close as possible. (See loop #1 of Figure 24)
  - The second important loop is the path from the low-side MOSFET through inductor and V_{OUT} capacitor(s), and back to source of the low-side MOSFET through ground. Connect source of the low-side MOSFET and negative node of V_{OUT} capacitor(s) at ground as close as possible. (See loop #2 of Figure 24)
  - The third important loop is of gate driving system for the low-side MOSFET. To turn on the low-side MOSFET, high current flows from V5IN capacitor through gate driver and the low-side MOSFET, and back to negative node of the capacitor through ground. To turn off the low-side MOSFET, high current flows from gate of the low-side MOSFET through the gate driver and GND pad of the device, and back to source of the low-side MOSFET through ground. Connect negative node of V5IN capacitor, source of the low-side MOSFET and GND pad of the device at ground as close as possible. (See loop #3 of Figure 24)

- Since the TPS51217 controls output voltage referring to voltage across V_{OUT} capacitor, the top-side resistor of the voltage divider should be connected to the positive node of V_{OUT} capacitor. In a same manner both bottom side resistor and GND pad of the device should be connected to the negative node of V_{OUT} capacitor. The trace from these resistors to the VFB pin should be short and thin. Place on the component side and avoid via(s) between these resistors and the device.
- Connect the overcurrent setting resistors from TRIP pin to ground and make the connections as close as possible to the device. The trace from TRIP pin to resistor and from resistor to ground should avoid coupling to a high-voltage switching node.
- Connections from gate drivers to the respective gate of the high-side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65 mm (25 mils) or wider trace and via(s) of at least 0.5 mm (20 mils) diameter along this trace.
- The PCB trace defined as switch node, which connects to source of high-side MOSFET, drain of low-side MOSFET and high-voltage side of the inductor, should be as short and wide as possible.

LAYOUT CONSIDERATIONS TO REMOTE SENSING

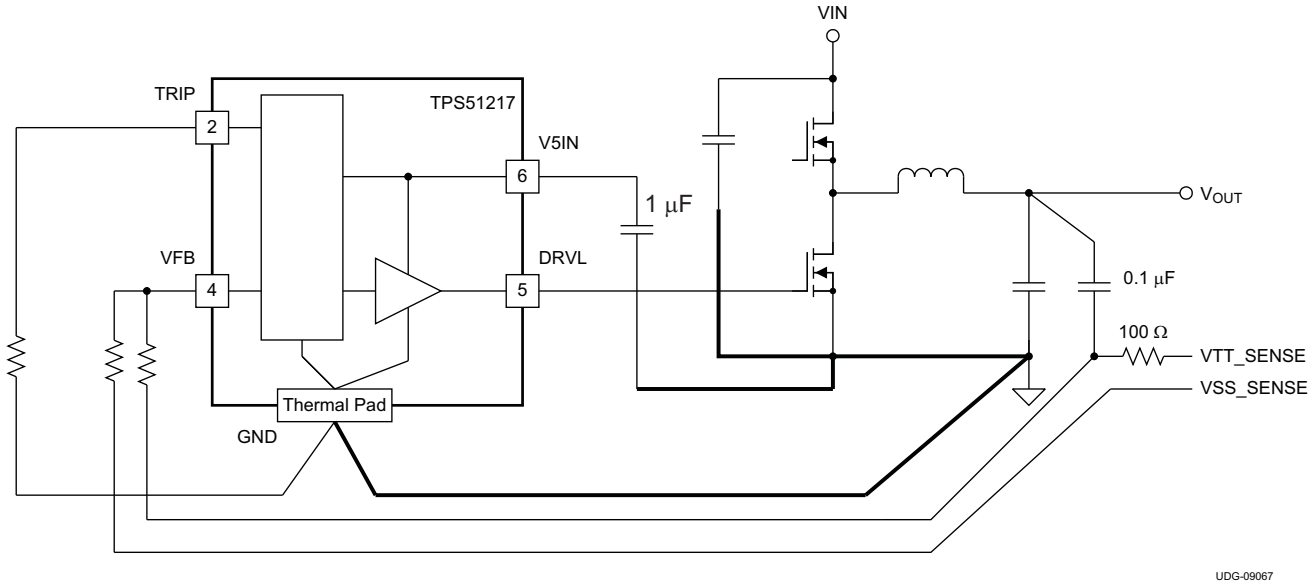


Figure 25. Remote Sensing of Output Voltage Using the TPS51217

- Make a Kelvin connection to the load device.
- Run the feedback signals as a differential pair to the device. The distance of these parallel pair should be as short as possible.
- Run the lines in a quiet layer. Isolate them from noisy signals by a voltage or ground plane.

TPS51217 APPLICATION CIRCUIT

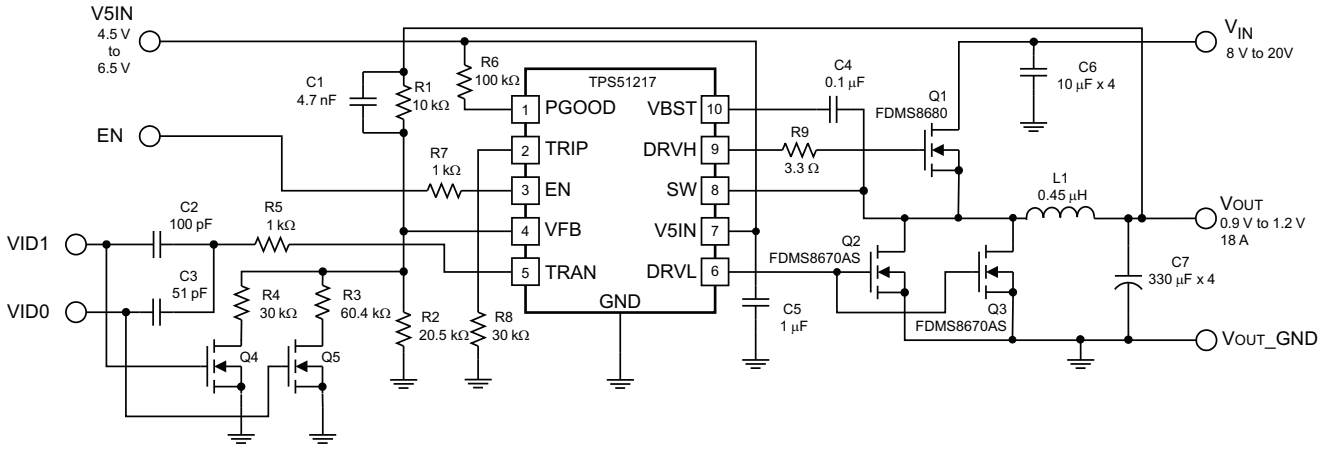


Figure 26. 0.9-V to 1.2-V/18A Auto-skip mode

Table 1. 0.9-V to 1.2-V/18A Application List of Materials

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C6	1	4 × 10 µF, 25 V	Taiyo Yuden	TMK325BJ106MM
C7	1	4 × 330 µF, 2 V, 12 mΩ	Panasonic	EEFCX0D331XR
L1	1	0.45 µH, 25 A, 1.1 mΩ	Panasonic	ETQP4LR45XFC
Q1	1	30 V, 35 A, 8.5 mΩ	Fairchild	FDMS8680
Q2, Q3	2	30 V, 42 A, 3.5 mΩ	Fairchild	FDMS8670AS

REVISION HISTORY

Changes from Original (June 2009) to Revision A **Page**

- Added text - Connect a 1-kΩ resistor in series with the EN pin to provide protection. To the ENABLE AND SOFT START section. 12

Changes from Revision A (August 2009) to Revision B **Page**

- Added DRVH specification to the ABSOLUTE MAXIMUM RATINGS table for pulse width < 20 ns 2
- Added DRVL specification to the ABSOLUTE MAXIMUM RATINGS table for pulse width < 20 ns 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51217DSCR	ACTIVE	WSON	DSC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PIYI	Samples
TPS51217DSCT	ACTIVE	WSON	DSC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PIYI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

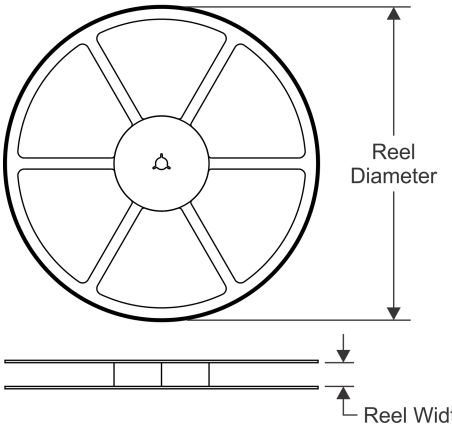
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

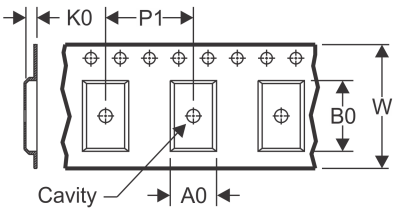
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

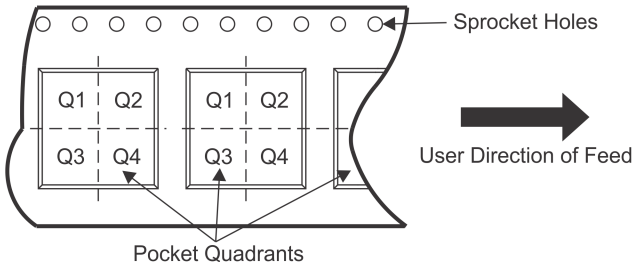


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

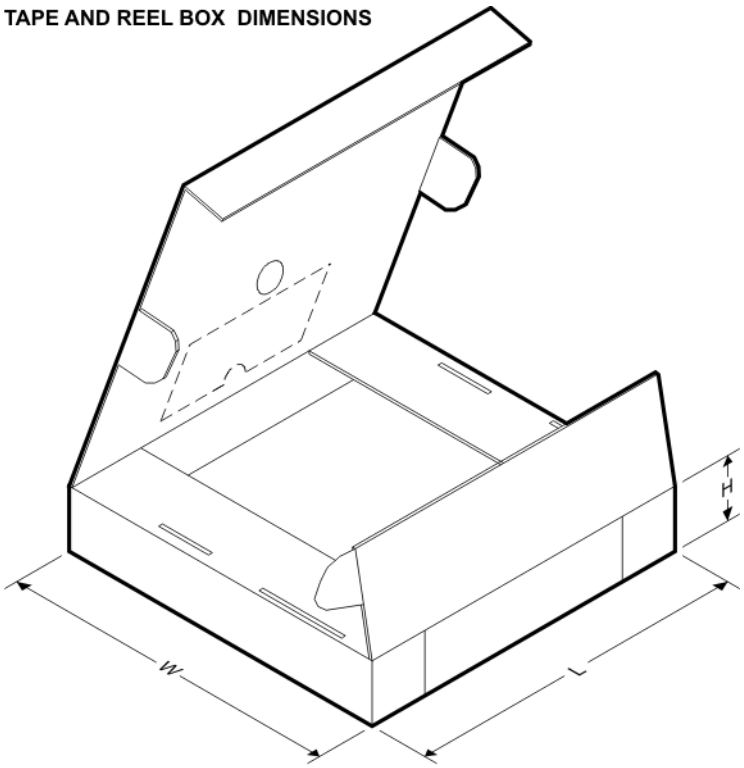
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51217DSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51217DSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51217DSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51217DSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

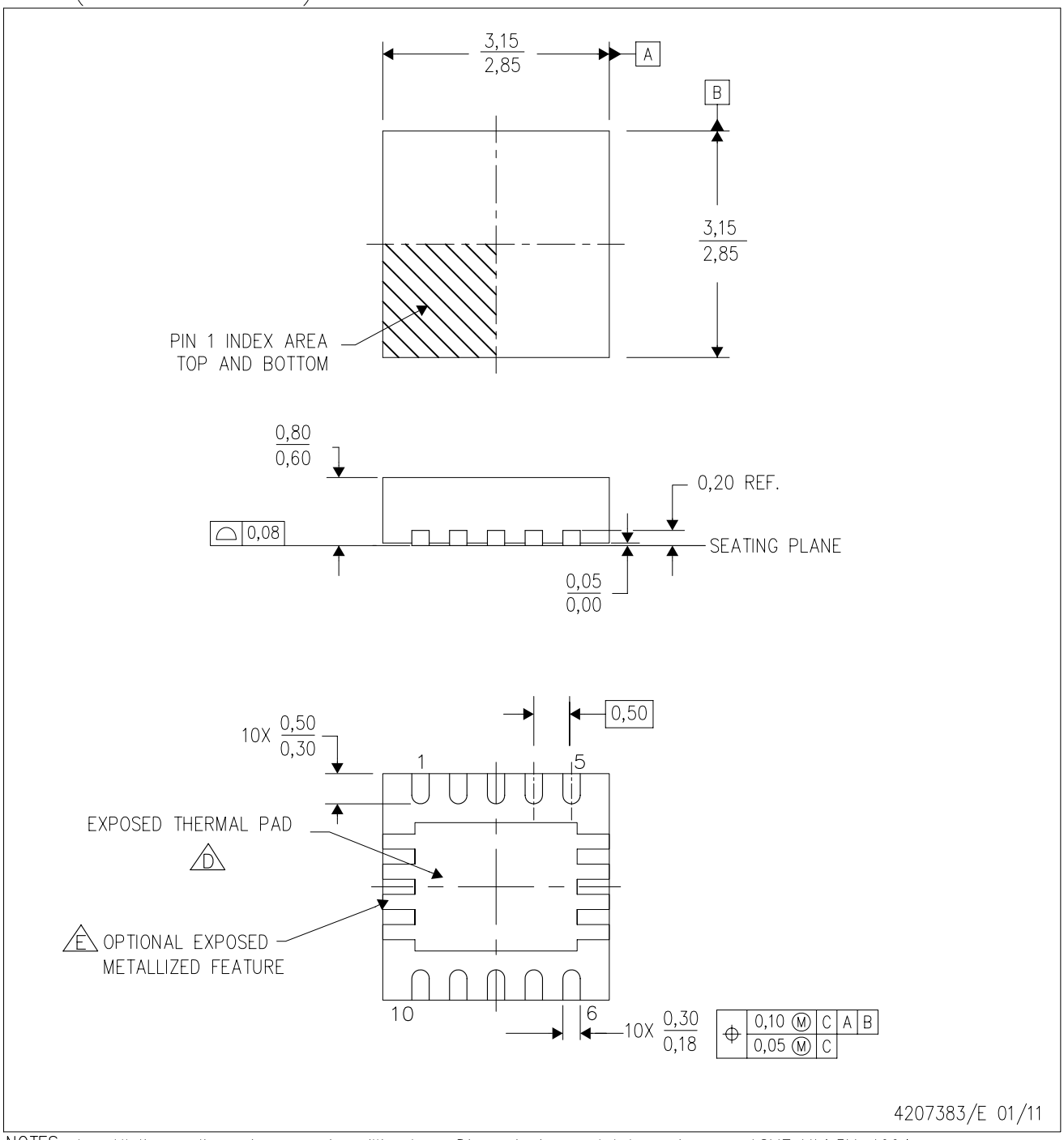
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51217DSCR	WSON	DSC	10	3000	367.0	367.0	35.0
TPS51217DSCR	WSON	DSC	10	3000	367.0	367.0	35.0
TPS51217DSCT	WSON	DSC	10	250	210.0	185.0	35.0
TPS51217DSCT	WSON	DSC	10	250	210.0	185.0	35.0

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

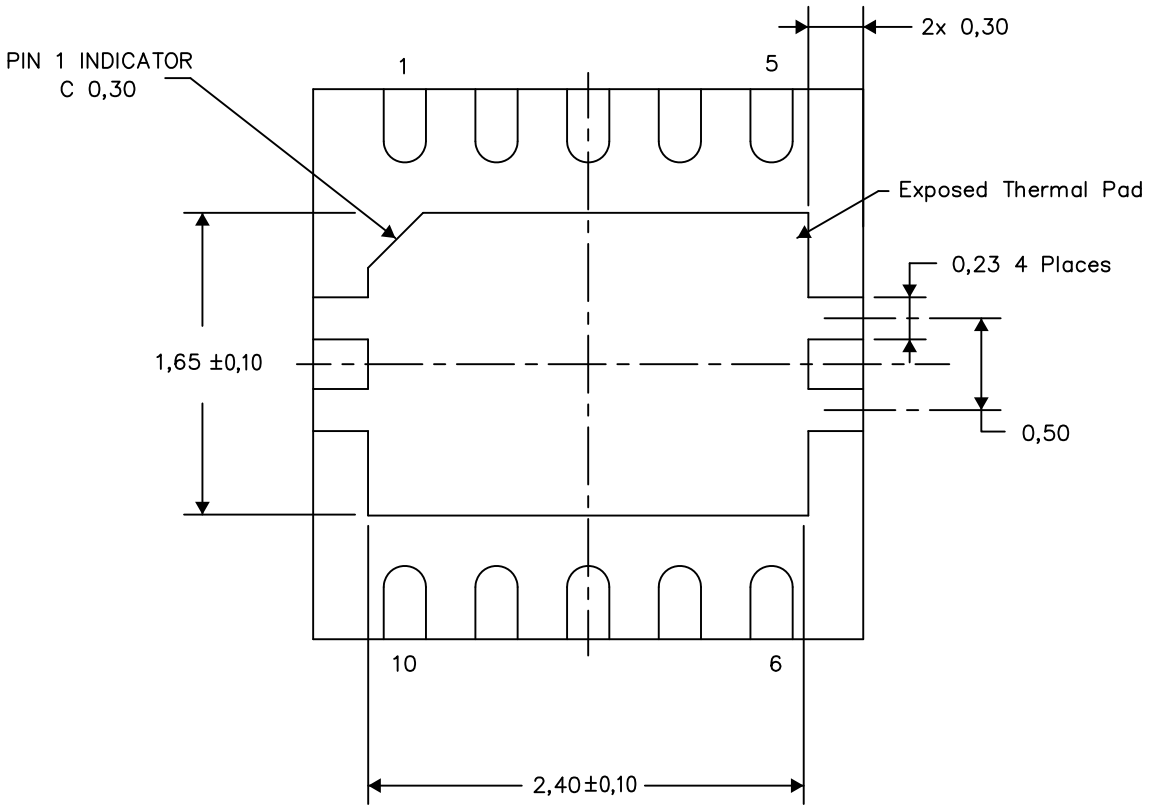
DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



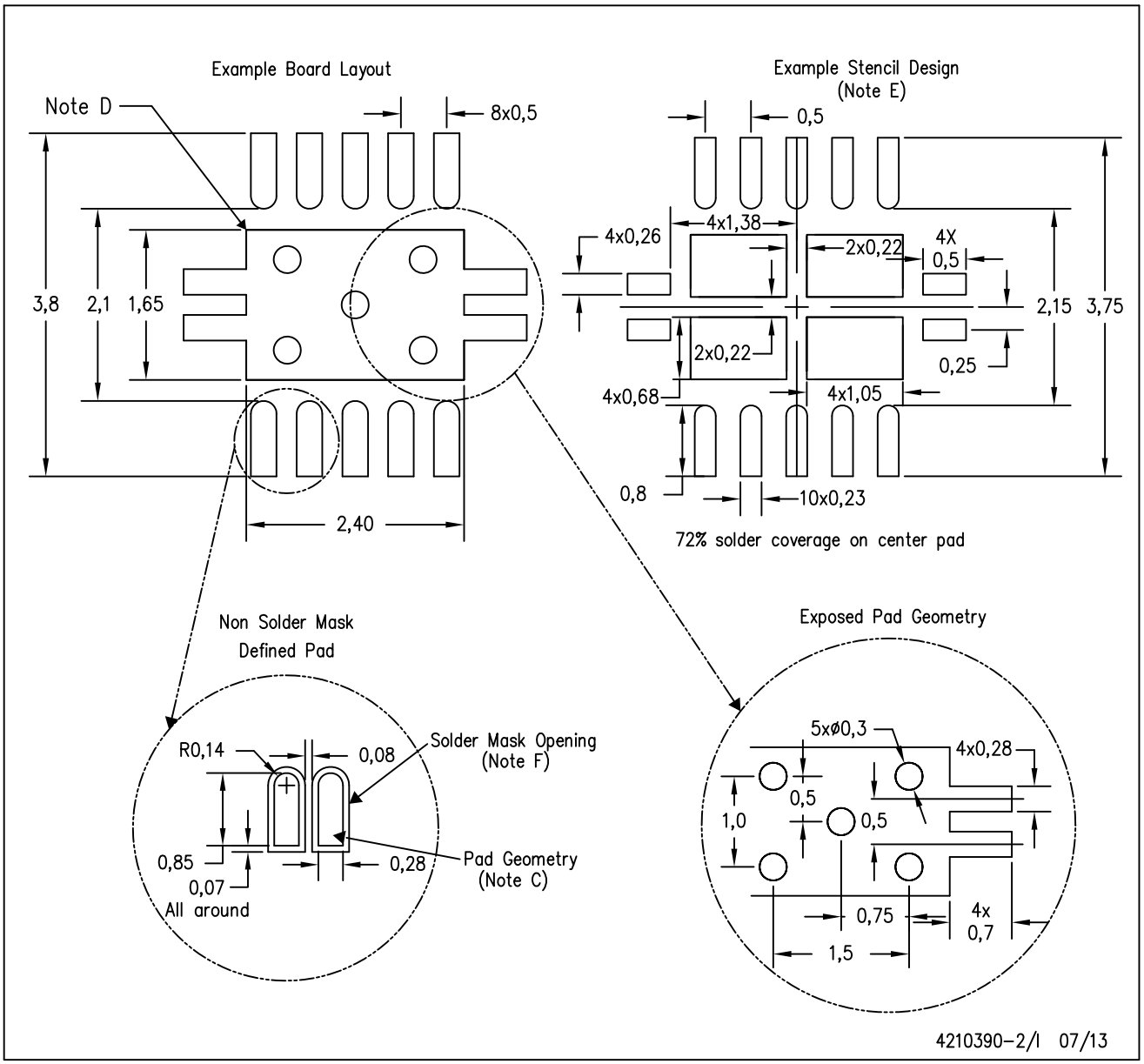
Bottom View

Exposed Thermal Pad Dimensions

4210391–2/M 08/13

NOTE: A. All linear dimensions are in millimeters

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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